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16. (Amended) The integrated edge structure according to claim 13, wherein each one of said at least two columns has a depth decreasing by shifting from said high voltage semiconductor device towards an outside of the integrated edge structure.

19. (Amended) The integrated edge structure according to claim 13, wherein said first conductivity type is N type and said second conductivity type is P type.

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20. (Amended) The integrated edge structure according to claim 13, wherein said first conductivity type is P type and said second conductivity type of conductivity is N type.

Please add the following claims 21-42:

21. (New) The integrated edge structure according to claim 13, wherein one or more doped regions of the at least two columns has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

22. (New) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar dopant concentration.

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23. (New) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar thickness.

24. (New) The integrated edge structure according to claim 13, wherein each of the at least two columns is spaced from any other of the at least two columns.

25. (New) An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the

region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed.

26. (New) The edge structure of claim 25, wherein each sub-region of each region is a doped semiconductor.

27. (New) The edge structure of claim 26, wherein each of the plurality of sub-regions of the plurality of regions has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

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28. (New) The edge structure of claim 25, wherein the edge structure further comprises:

a plurality of layers of a second conductivity type superimposed on one another,

wherein each region of the plurality of regions is disposed within at least two of the plurality of superimposed layers.

29. (New) The edge structure of claim 28, wherein each region of the plurality of regions is spaced from each of the other of the plurality of regions by portions of two or more of the plurality of superimposed layers.

30. (New) The edge structure of claim 28, wherein the plurality of superimposed layers is superimposed on a semiconductor substrate.

31. (New) The edge structure of claim 28, wherein the plurality of superimposed layers have a similar dopant concentration.

32. (New) The edge structure of claim 28, wherein the plurality of superimposed layers have a similar thickness.

33. (New) The edge structure of claim 25, wherein the semiconductor device is a high-voltage semiconductor device.

34. (New) The edge structure of claim 33, wherein the semiconductor device is a power MOSFET.

35. (New) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are merged together.

36. (New) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are not merged together.

37. (New) The edge structure of claim 25, wherein the first conductivity type is N type and the second conductivity type is P type.

38. (New) The edge structure of claim 25, wherein the first conductivity type is P type and the second conductivity type is N type.

39. (New) The edge structure of claim 25, wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

40. (New) The edge structure of claim 25, wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases curvature radii of equipotential lines associated with the edge portion of the depletion region.

41. The edge structure of claim 25, wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure decreases an electric field associated with the edge portion of the deletion layer.

42. The edge structure of claim 25, wherein the semiconductor device includes a PN junction

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having an associated depletion region including an edge portion and a plane portion, and

wherein the edge structure reduces a ratio of a breakdown voltage of the edge portion to a breakdown voltage of plane portion.